

Preface

In October 2001 the IBM eServer pSeries 690 was announced. The p690, known in development by the code name Regatta, introduced the POWER4 microprocessor to the high end of the UNIX market. It embraces the IBM eServer objectives. Initially targeted for the pSeries, the POWER4 will also be used in iSeries servers. This technology will be rapidly deployed in the midrange and low end of the pSeries and iSeries offerings. It is the fastest 64-bit microprocessor shipping in the industry today after being introduced at 1.3 GHz.

The POWER4 development project was a five-year effort from inception to volume shipment of systems, which began in December 2001. It is, however, more than a microprocessor. It is a total system including the supporting chip set and the software to support the systems using it. This was a complex project requiring many subsystem technologies to interoperate and come together. Five years ago, it was clear that IBM had very competitive technology. It was also clear, however, that the market for new systems was transforming into one in which e-business would dominate. This would require a new approach to servers. The development team was formed with people from all of the major IBM research and development laboratories. This allowed us to bring the best ideas from across all servers within IBM into a single project. We analyzed our design options and assessed what were acceptable risks. What resulted is the POWER4 microprocessor and technology. In this topical issue, we describe some of that technology and some aspects of the special development environment that was required to achieve the design and performance goals and bring POWER4 to market on schedule.

Throughout the development program, the focus was always on the entire system, leveraging one of IBM's strengths, its systems expertise. The IBM RISC System/6000 was introduced in 1990. In October 2000, IBM redefined its product line and introduced the eServer line of servers, featuring mainframe-class reliability and scalability, broad support of open standards for the development of new applications, logical partitioning to allow multiple virtual servers to coexist in a single physical system, and capacity on demand for managing the unprecedented demands of e-business. With that announcement, the RISC System/6000 was transformed into the pSeries, the most powerful, technologically advanced IBM UNIX server. Today, pSeries servers, as do all eServer servers, also embrace the Linux operating system.

The paper by Tendler et al. describes the POWER4 microarchitecture and the microarchitecture of systems based on the POWER4 microprocessor. This technology is first being offered in the pSeries, but the description is valid for future systems as well, since the POWER4 will

be used across the entire pSeries and iSeries line over time. The technology introduced with the current offering is applicable to both commercial and technical applications. Features incorporated in the design to allow superior performance in both of these markets are described here. As is the case with all of the papers in this issue, a system view is taken, not just one of describing the microprocessor.

A chip operating at more than 1 GHz that includes two processors, together with cache and switching circuitry, that is built with 174 million transistors interconnected with more than a mile of wiring, and that is implemented in state-of-the-art technology, requires a new methodology in addressing the circuitry used and in the layout of the chip. Additionally, off-chip buses were specified as operating at half the processor frequency and scaling with processor frequency, further complicating the technical challenge. In the initial POWER4 implementation, this meant that inter-chip buses had to operate at speeds up to 650 MHz, both on and off the module holding the chips. This had never been done previously. Adding to that the absolute requirement of maintaining schedule with a multi-site development team made an already difficult task even more challenging. The paper by Warnock et al. describes the approach used and the results achieved. They describe the design methodology, clock distribution, circuits, power, integration, and timing that enabled the design team to meet the project goals.

A major challenge for many projects that introduce a new design, such as this one, often is the verification effort. In our case, this was further compounded by our desire to introduce the high end of the line initially. Most development programs have done the opposite, but in our view, servers meant that we needed to offer a large, symmetric multiprocessing system, and had to ensure that it would work from the very beginning. We could not afford the cost to redo the design if we later found some major flaws. The paper by Ludden et al. describes the approach we used. The verification approach used was a hierarchical one, enhancing and expanding on what was previously used to verify the S/390 Parallel Enterprise Server G4 system. The verification task was further complicated by the out-of-order design of the microprocessor. This dictated a multifaceted approach that is described in their paper.

As our economy becomes one that embraces e-business, the demand for reliability increases. For the POWER4 project, we needed to accelerate the introduction into UNIX servers of the reliability, availability, and serviceability features which we pioneered on IBM mainframes. The paper by Bossen et al. describes how POWER4-based systems achieve high availability designed into the system from the outset. Fault-tolerant design techniques used throughout are highlighted. To improve

the diagnostic strategy, fault isolation and recovery techniques are described. The total system design employed throughout the project is evident in the approach used, in which many of the higher-reliability features require the hardware, firmware, and software to act together.

A project that is geographically dispersed across multiple sites on an aggressive schedule also requires an innovative approach to project management and the infrastructure used to support the project. The paper by Rodgers et al. describes the development project infrastructure. Without this in place, the project would never have come close to delivering on a schedule established five years in advance.

The POWER4 development program has met all of its design and performance goals and was completed on schedule. This achievement reflects the effort not only of the authors whose work is reported here, but also of a great many people at all of the major development locations of the IBM Server Group. I am very pleased to acknowledge their dedication and commitment.

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